Cost-Effective Chip-On-Heat Sink Leadframe Package for 800-Mb/s/Lead Applications

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***Abstract*—Chip-on-heat sink leadframe (COHS-LF) packages offer a simple, low-cost chip encapsulation structure with advanced electrical and thermal performance for high-speed integrated circuit applications. The COHS-LF package is a novel solution to the problems of increased power consumption and signal bandwidth demands that result from high-speed data transmission rates. Not only does it offer high thermal and electrical performance, but also provides a low-cost short time-to-market package solution for high-speed applications. In general, there are two main memory packages employed by the most popular high-speed applications, double data rate (DDR) SDRAM. One is the cheaper, higher parasitic leadframe packages, such as the thin small outline packages (TSOPs), and the other is the more expensive, lower parasitic substrate-based packages, such as the ball grid array (BGA). Due to the requirement for higher ambient temperature and operating frequency for high-speed devices, DDR2 SDRAM packages were switched from conventional TSOPs to more expensive chip-scale packages (i.e., BGA) with lower parasitic effects. And yet, by using an exposed heat sink pasted on the surface of the chip and packed in a conventional leadframe package, the COHS-LF is a simpler, lower cost design. Results of a three-dimensional full-wave electromagnetic field solver and SPICE simulator tests show that the COHS-LF package achieves less signal loss, propagation delay, edge rate degradation, and crosstalk than the BGA package. Furthermore, transient analysis using the wideband T-3π models optimized up to 5.6 GHz for signal speeds as high as 800 Mb/s/lead demonstrates the accuracy of the equivalent circuit model and reconfirms the superior electrical characteristics of COHS-LF package.**

***Index Terms*—Ball grid array (BGA), chip-on-heat sink leadframe (COHS-LF), crosstalk, exposed heat sink, rise time, S-parameters, SPICE, thin small outline packages (TSOPs).**

I. Introduction

THERE ARE two main packaging challenges encountered with high-speed data transmission. One is that more power consumption induces thermal problems, and the other is that higher signal bandwidth results in electrical problems. Packages with lower parasitic effects, such as ball grid arrays (BGAs), can accommodate increases in power consumption and higher signal bandwidths, but are more costly than packages that do not perform as well in high-speed data applications, like thin small outline packages (TSOPs). Therefore, packaging with *both* lower parasitic effects and lower costs is needed for high-speed integrated circuit applications. This paper proposes the chip-on-heat sink leadframe (COHS-LF) package as a novel solution that meets the low-cost, high-performance criteria of high-speed applications.

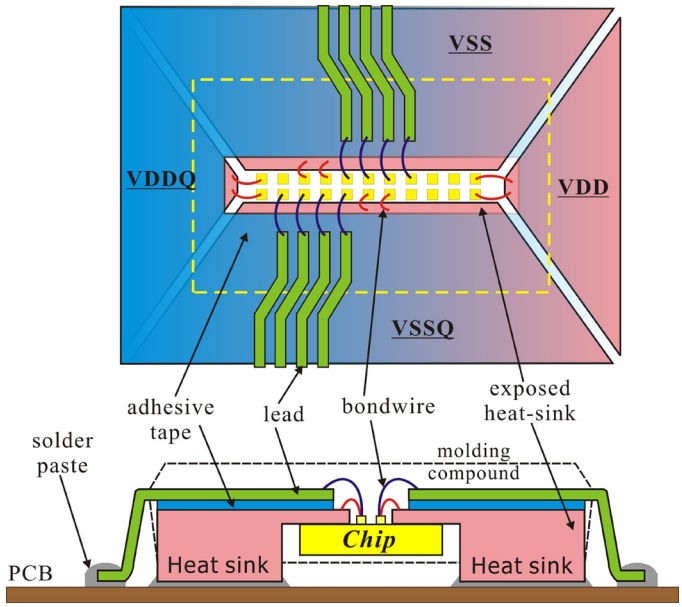

Fig. 1. COHS-LF package top and cross-sectional views. (Color version available online at http://ieeexplore.ieee.org.)

The organization of this paper includes the COHS-LF package structure and lead impedance design, a performance comparison among packages, and a transient analysis for high-speed signal (400 to 800 Mb/s/lead) applications. Performance comparisons include a three-dimensional (3-D) finite-element analysis (FEA) program to evaluate thermal performance, a comparison of high-frequency characteristics of the COHS-LF and TSOP packages, and S-parameter and transient simulation with wideband T-3π equivalent circuit model comparisons of the COHS-LF and BGA packages.

II. Package Structure and Impedance Design

Fig. 1 shows the proposed COHS-LF package. The COHS-LF package is similar to the lead-on-chip TSOP (LOC-TSOP), with the exception of the additional, exposed heat sink between the leadframe and the chip using adhesive tape.

Due to the similarity, the COHS-LF package can be assembled using existing standards and processes, as shown in Fig. 2. The *only* additional procedure required is that the heat sink is

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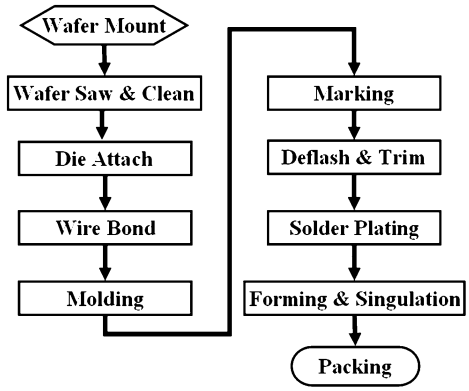

Fig. 2. Standard process flow of leadframe packages.

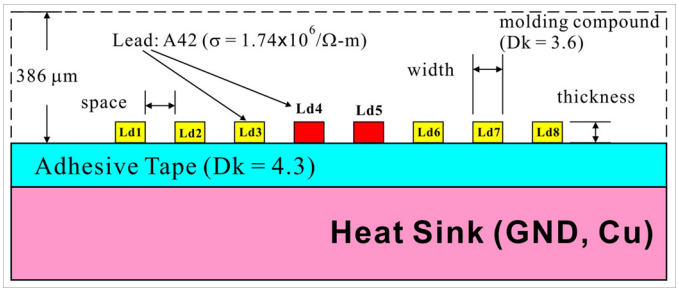

Fig. 3. Cross section of COHS-LF package for 50-Ω impedance per lead. (Color version available online at http://ieeexplore.ieee.org.)

attached to the leadframe using adhesive tapes before the die is attached ("die attach"). The added heat sink not only improves heat removal, but also creates several power and ground planes. These power and ground planes are bonded to the corresponding power and ground pads on the die and then soldered to the power and ground nets on the printed circuit board (PCB). Since power and ground do not need to go through the leads on the COHS-LF package, there is more space available to design the lead geometry for high-speed applications, and therefore increased opportunity to reduce the package size.

The grounded heat sink beneath the leads allows for controlling the impedance. Fig. 3 shows the package and lead geometry, as well as the materials. When grounding the leads to the surrounding target leads (Leads 4 and 5), a simulation at 100 MHz using the Ansoft Maxwell 2-D Quick Parameter Extractor shows an impedance of 51.3 Ω when using 0.6-mm lead space, 0.18-mm lead width, 0.127-mm lead thickness, and 0.14-mm adhesive tape thickness.

III. Comparison of Package Performance

A. Thermal Performance

Heat flows from the higher temperature chip to the lower temperature ambient environment. Therefore, a higher thermal conductivity (k) between chip and ambient will enhance heat removal (e.g., copper $k \approx 400$ W/mK°). Fig. 4 shows a comparison of the major heat flow paths for the BGA, LOC-TSOP, and COHS-LF packages. As compared to the LOC-TSOP and BGA packages, a higher efficiency of thermal removal for the COHS-LF is expected due to the higher thermal conductivity of the copper heat sink. However, to further evaluate heat removal

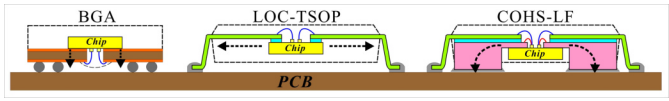

Fig. 4. Major heat flow path for BGA, LOC-TSOP, and COHS-LF packages. (Color version available online at http://ieeexplore.ieee.org.)

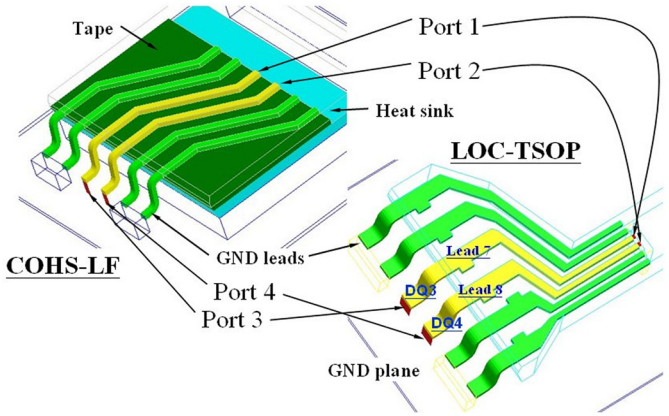

Fig. 5. 3-D structures for COHS-LF and LOC-TSOP packages. (Color version available online at http://ieeexplore.ieee.org.)

performance between the BGA and COHS-LF packages, the junction to ambient thermal resistance (θ_{ja}) was simulated using ANSYS with the package soldered on the JEDEC higher conduction 4L board in a standstill atmosphere [1]. Simulated junction to ambient thermal resistance for the COHS-LF, BGA, and LOC-TSOP packages showed 47.6, 54.4, and 74.2°C/W, respectively. The temperature increment between the BGA and LOC-TSOP is expected. Thermal analysis of the COHS-LF package shows it has an even smaller temperature increment than the BGA package (as well as the LOC-TSOP).

B. Electrical Performance—COHS-LF and LOC-TSOP Packages

The 3-D structures used in Ansoft HFSS for the COHS-LF and LOC-TSOP54 packages are shown in Fig. 5. Both packages have the same size, lead, and dielectric materials [2]. It can be observed that equal lead width and space in the COHS-LF package may result in nearly constant impedance for each lead, whereas the LOC-TSOP does not have these features and heat sink reference plane. Two leads, Lead 7 (DQ3) and Lead 8 (DQ4), without bond wires, were selected as a four-port network for comparison. The PCB ground plane was 0.142 mm below the package [3]. The leads surrounding Leads 7 and 8 were grounded. Each signal port was terminated to a 50-Ω load. Fig. 6 shows the S-parameters from 0.1 to 12 GHz for both packages. Results show that the COHS-LF package has less energy loss and coupling compared with the LOC-TSOP.

C. Electrical Performance in Frequency Domain—COHS-LF and BGA Packages

The BGA package featured with a center slot is suitable for chips with pads at the center, such as DRAMs. Therefore, the bondwires can be as short as 1 mm. Table I shows the detailed package information. Fig. 7 shows the 3-D models established in Ansoft HFSS for the COHS-LF and two-layer BGA packages,

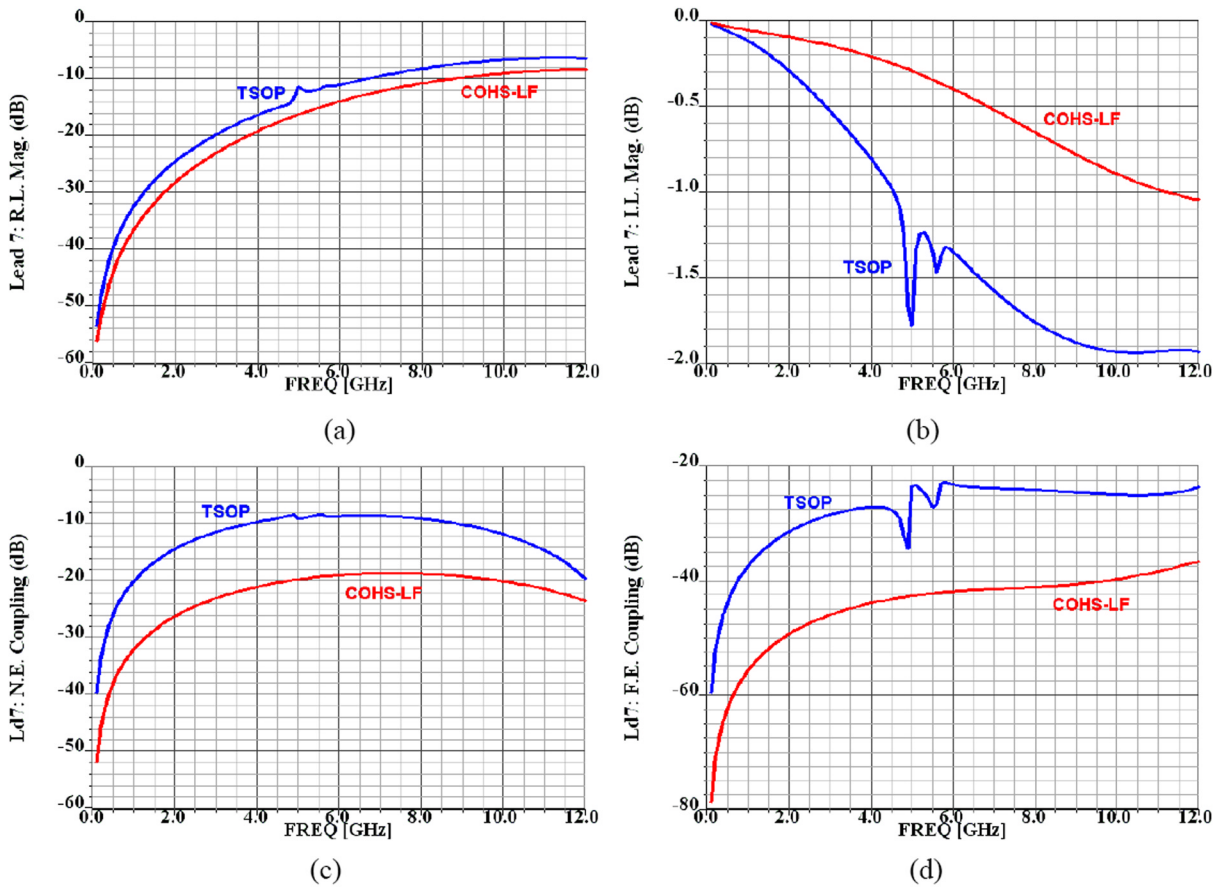

Fig. 6. Comparison of S-parameter in magnitude between COHS-LF and LOC-TSOP. (a) Return loss of Lead 7 (S_{11}). (b) Insertion loss of Lead 7 (S_{31}). (c) Near-end coupling of Lead 7 (S_{21}). (d) Far-end coupling of Lead 7 (S_{41}). (Color version available online at http://ieeexplore.ieee.org.)

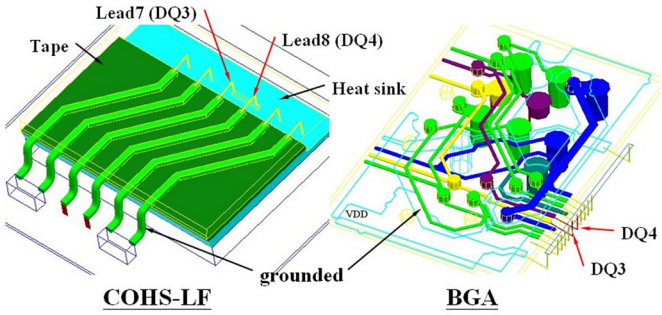

Fig. 7. 3-D structures for COHS-LF and BGA packages. (Color version available online at http://ieeexplore.ieee.org.)

per the EIA/JEDEC standard [4]. The two leads (traces), Lead 7 (DQ3) and Lead 8 (DQ4), with bond wires, were selected as a four-port network for comparison. Each signal port was terminated to a 50-Ω load. Port 1 and Port 2 were assigned at the wire sides, while Port 3 and Port 4 were at the external lead ends or ball ends. A PCB ground plane was also placed at 0.142 mm below the package. The leads or traces surrounding Lead 7 (or DQ3) and Lead 8 (or DQ4) were grounded. Fig. 8 shows the S-parameters from 0.1 to 12 GHz for both packages. In general, the energy losses and coupling of the COHS-LF package are less than those of BGA package within 12 GHz. This is due to the limitation of the BGA package structure using plating lines, multivia-holes, and no solid reference plane in the package to control impedance and suppress signal coupling.

D. Electrical Performance in Time Domain—COHS-LF and BGA Packages

Clock frequency is increasing for many digital circuit applications. In fact, DDR2 DRAMs, for example, will reach 800 Mb/s per net in the near future. Since the signal pulse is composed of many higher frequency components, a wideband equivalent circuit model is required to evaluate the transient behavior of the package. For an 800-Mb/s pulse with signal swing (Vin) from 0 to 1.8 V and 45% duty cycle, the rise time (T_r, 10–90%) and fall time (T_f, 90%–10%) are assumed to be 62.5 ps. The 3-dB bandwidth $(F_{3\text{dB}})$ is $0.35/T_r = 5.6$ GHz. Since the longest transmission line in the COHS-LF and BGA package is 7.64 mm, the critical length, one tenth of the wavelength in the package calculated using the parameters in Table I, is about 2.58 mm [5]. The number of *RLCG* segments is $7.64/2.58 \approx 3$, where one segment of π-model is shown in Fig. 9(a).

Many studies in package characterization [6]–[12] neglected the capacitance effects in the bondwire electrical model. This resulted in poor agreement between the wideband electrical model and S-parameters of the package. Due to the inductive bondwires, an additional T-model for the bondwire capacitance effects is in series with three cascaded π-models, as shown in Fig. 9(b). The T-3π model is shown in Fig. 9(c).

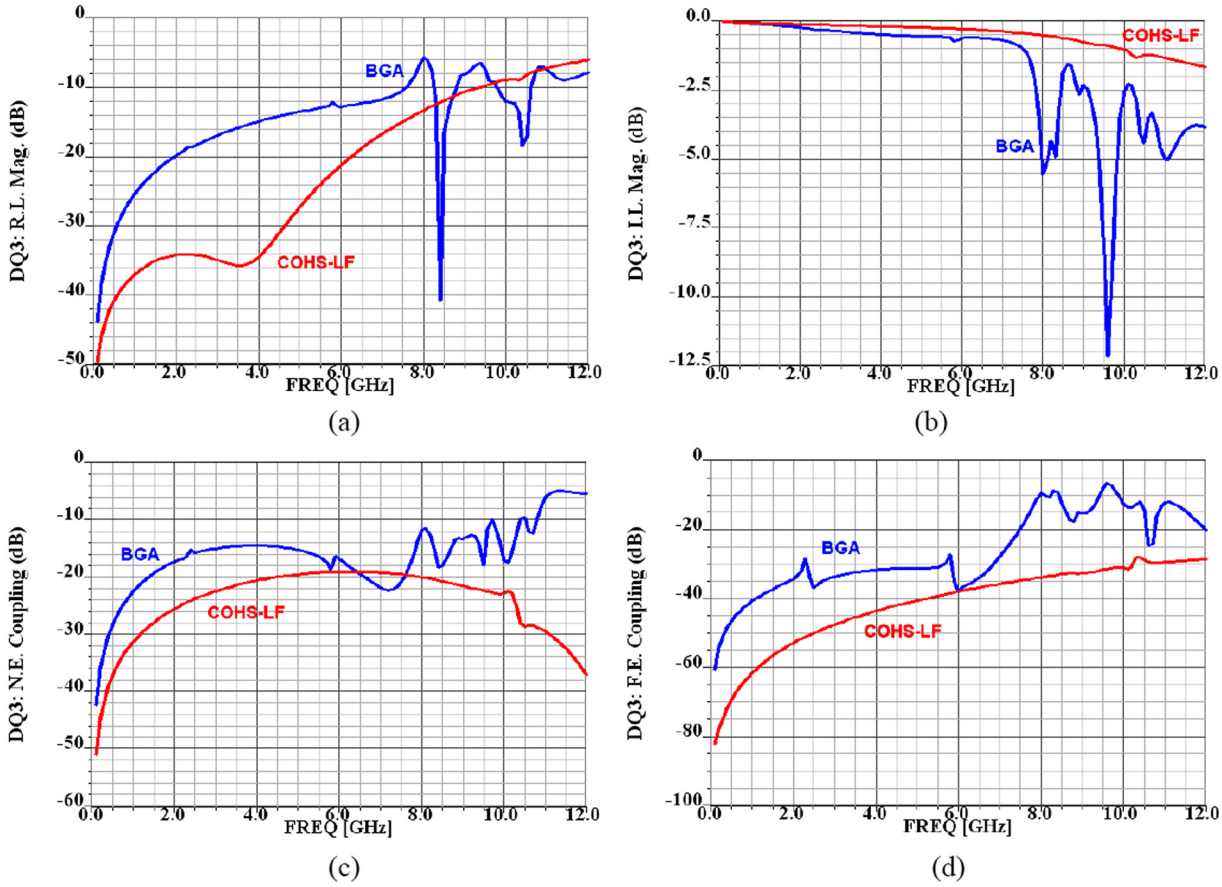

Fig. 8. Comparison of S-parameter in magnitude between the COHS-LF and BGA packages. (a) Return loss of Lead 7/DQ3 (S_{11}). (b) Insertion loss of Lead 7/DQ3 (S_{31}). (c) Near-end coupling of Lead 7/DQ3 (S_{21}). (d) Far-end coupling of Lead 7/DQ3 (S_{41}). (Color version available online at http://ieeexplore.ieee.org.)

TABLE I
DETAILED PACKAGE INFORMATION

Item	COHS-LF	BGA
Package size (LxWxH)	11.8 x 22.2 x 1.1 mm^3	9 x 13 x 0.476 mm^3
Lead or Ball count	54	54
Lead or Ball pitch	0.78 mm	0.80 mm
Lead or Trace material	A42 (σ = 1.74 x 10^6 /Ω-m)	Copper (σ = 5.8 x 10^7 /Ω-m)
Lead or Trace: width/space/ thickness	180/600/127 μm	60/65/23 μm
Gold-wire diameter	1.2 mil	0.8 mil
Wire length/Loop height	0.62/0.36 mm	0.6/0.37 mm
Molding compound	D_k = 4.3, D_f = 0.006	D_k = 4.1, D_f = 0.01
Tape or BT material/thickness	HM-122U-F/0.14 mm (D_k = 3.13, D_f = 0.008)	HL-832/0.15 mm (D_k = 4.2, D_f = 0.012)
Solder mask	N/A	D_k = 4.0, D_f = 0.028
Inner lead or trace length	4.27 mm	DQ3: 4.88 mm DQ4: 6.67 mm
Outer lead or plating line length	1.49 mm	DQ3: 2.79 mm DQ4: 0.72 mm
Via length/Ball height	N/A	0.15/0.28 mm

The minimum serial resistance, R_{w1}, R_{w2}, R_{i1}, and R_{i2}, together with the maximum parallel resistance (RL_{w1}, RL_{w2}, RL_{i1}, and RL_{i2}) in the equivalent circuit model can match the signal responses reasonably well over a wide frequency range

TABLE II
LUMPED PARASITIC PARAMETERS OF T-3π MODEL FOR COHS-LF AND BGA PACKAGES

Package Type	Net Name	R_{lump} (Ω)	Ls_{lump} (nH)	Lm_{lump} (nH)	Co_{lump} (pF)	Cm_{lump} (pF)	G_{lump} ($m\Omega^{-1}$)	Zo (Ω)
BGA	DQ3	0.733	3.390	0.687	0.805	0.211	0.26	57.8
	DQ4	0.795	3.642		0.772		0.31	60.9
COHS-LF	Lead7	0.398	2.161	0.224	0.713	0.095	0.07	51.7
	Lead8	0.393	2.098		0.761		0.06	49.5

[13]–[14]. The optimized parasitic parameters of both packages were obtained using the Ansoft Harmonica. Fig. 10 shows some of the S-parameters generated by Ansoft HFSS and the wideband equivalent circuit model for the COHS-LF and BGA packages. It can be observed that the curves are well matched, and the optimized parasitic parameters of the equivalent circuit are reliable up to 5.6 GHz. The lumped parasitic parameters and the characteristic impedance (Zo) of the T-3π model are listed in Table II, where R, Ls, Lm, Co, Cm, G, and Zo are resistance, self inductance, mutual inductance, SPICE capacitance, mutual capacitance, conductance, and characteristic impedance for each lead or trace, respectively. Zo of the COHS-LF package nearly agrees with the impedance design described in Section II. It is consistent with the smaller return loss due to smaller Zo deviation from 50 Ω.

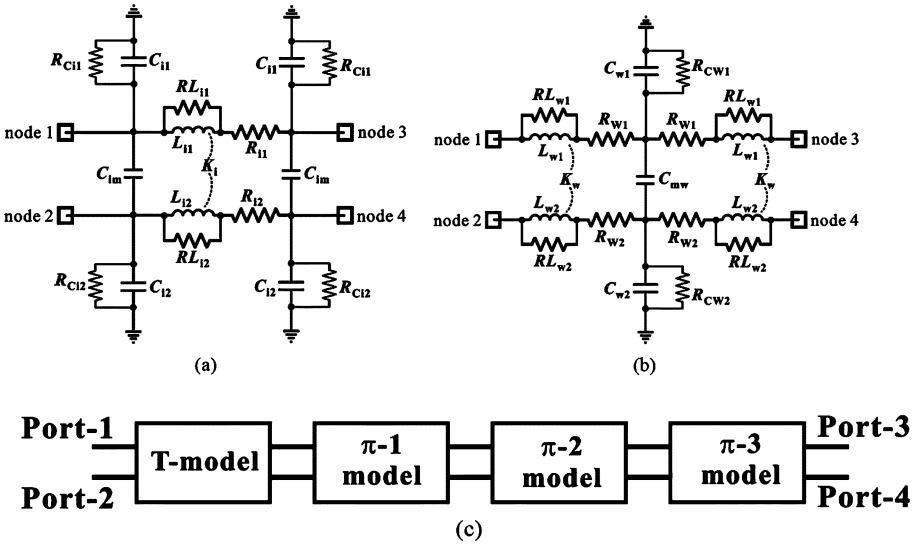

Fig. 9. Wideband equivalent circuit using T-3π model. (a) One section of π-model, $i = 1$, 2, and 3. (b) T-model. (c) The T-3π model is consisted of a T-model in series with three cascaded π-models.

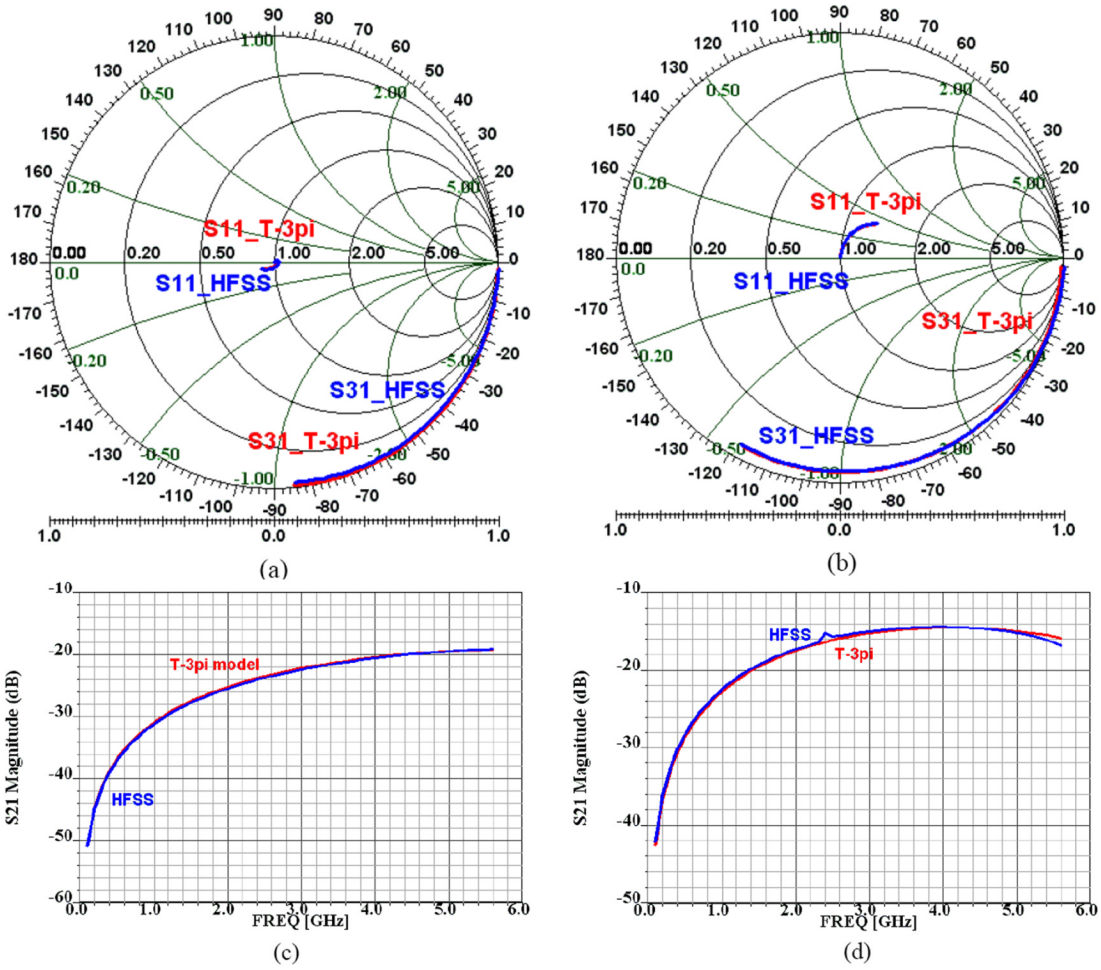

Fig. 10. S-Parameters generated from Ansoft HFSS and wideband T-3π equivalent circuit model. Data agrees up to 5.6 GHz. Smith chart of S_{11} and S_{31}. (a) COHS-LF package. (b) BGA package. S_{21} magnitude chart (c) COHS-LF package. (d) BGA package. (Color version available online at http://ieeexplore.ieee.org.)

The parasitic parameters optimized from the Ansoft Harmonica were used in SPICE simulations for transient analyses. Fig. 11 shows the transient responses of the COHS-LF and BGA packages. Both the input and output terminals of the

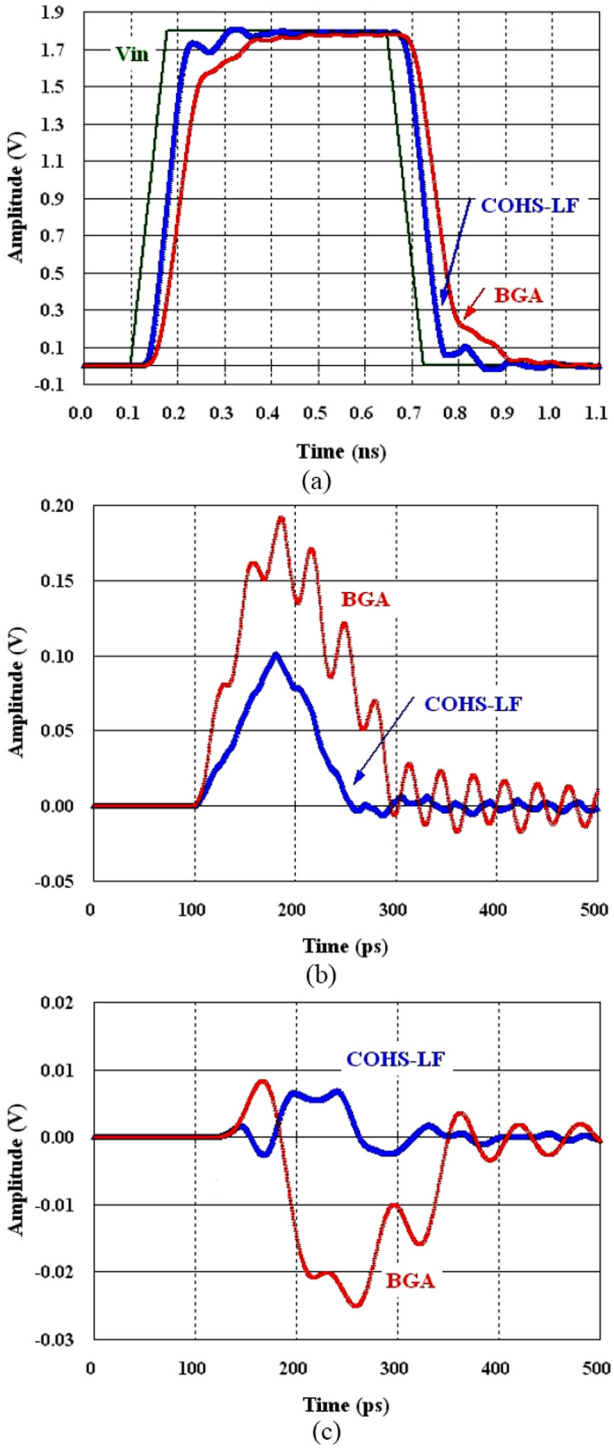

Fig. 11. Transient analyses for COHS-LF and BGA packages. (a) Input (Vin) and output waveforms of Lead 7 (COHS-LF package) and DQ3 (BGA package). (b) Near-end crosstalk of Lead 8 (COHS-LF package) and DQ4 (BGA package). (c) Far-end crosstalk of Lead 8 (COHS-LF package) and DQ4 (BGA package). (Color version available online at http://ieeexplore.ieee.org.)

active and quiet lines were connected to 50-Ω loads. Refer to Section III-D for an explanation of the input waveform (Vin). In Fig. 11(a), the edge rate of output waveform for the BGA package is degraded. The corners at the rising and falling edges cannot be varied rapidly. This phenomena results from the larger product of inductance and capacitance, which acts as a low-pass filter to filter out some of the high-frequency components of the input signal. The voltage waveforms of near-end (NE) and far-end (FE) crosstalk (XT) are shown in Fig. 11(b) and (c). The larger NEXT and FEXT in the BGA package are due to the larger Cm and Lm. The measured output delay, T_r, T_f, NEXT, and FEXT are summarized in Table III. The percentage values at the NEXT and FEXT represent the maximum peak crosstalk divided by the amplitude of signal. In summary, the electrical performance of COHS-LF package is better than that of BGA package.

IV. High-Speed Applications

Theoretically, the wideband T-3π model should be accurate for pulse speeds below 800 Mb/s, since it was optimized up to 5.6 GHz. Fig. 12 shows the simulated voltage waveforms of near-end and far-end crosstalk for 400, 533, 667, and 800 Mb/s signals with corresponding rise time (T_r) of input signal (Vin), as defined in Table IV. The 800 Mb/s signal gives the highest peak values due to its shortest rise time. Table IV also summarizes the corresponding time delays (TD), NEXTs and FEXTs for Lead 8 with the active signal at Lead 7 of the four data speeds measured from the SPICE simulation. The time delays for data speeds from 400 to 800 Mb/s are around 40 ps, which is almost independent of the signal rise time.

V. Conclusion

A cost-effective, high-performance COHS-LF package with well-controlled impedance is proposed for applications with data speeds requirements up to 800 Mb/s. The S-parameters and transient analyses using wideband T-3π equivalent circuit models optimized up to 5.6 GHz were performed for the BGA and COHS-LF packages. The BGA package showed larger parasitic inductance and capacitance resulting in both a larger propagation delay and degradation of the edge rate by filtering out some of high-frequency components. Unlike the COHS-LF package, the structure of the BGA package is the limiting factor for enhanced electrical performance. A two-layer substrate with plating lines is used in the BGA package, where some signal traces require multivia holes for routing. The plating line and via holes produce impedance discontinuity, which is adverse for high-speed applications. It is also difficult to add a solid reference plane to the two-layer BGA package and control of the trace impedance and reduction of coupling is hardly feasible.

This makes the COHS-LF superior to the BGA package for 800 Mb/s applications. Not only does the exposed heat sink in the COHS-LF leadframe package help remove heat generated by the chip, it also reduces parasitic effects for signal loss, delay, edge rate degradation, and crosstalk. Furthermore, because the only additional procedure required during assembly is to attach the heat sink to the leadframe using adhesive tapes, the COHS-LF package can be assembled using existing standards and processes, keeping costs down and time-to market short. In summary, the COHS-LF package is a simple low-cost structure with high electrical and thermal performance that meets short time-to-market requirements for high-speed applications.

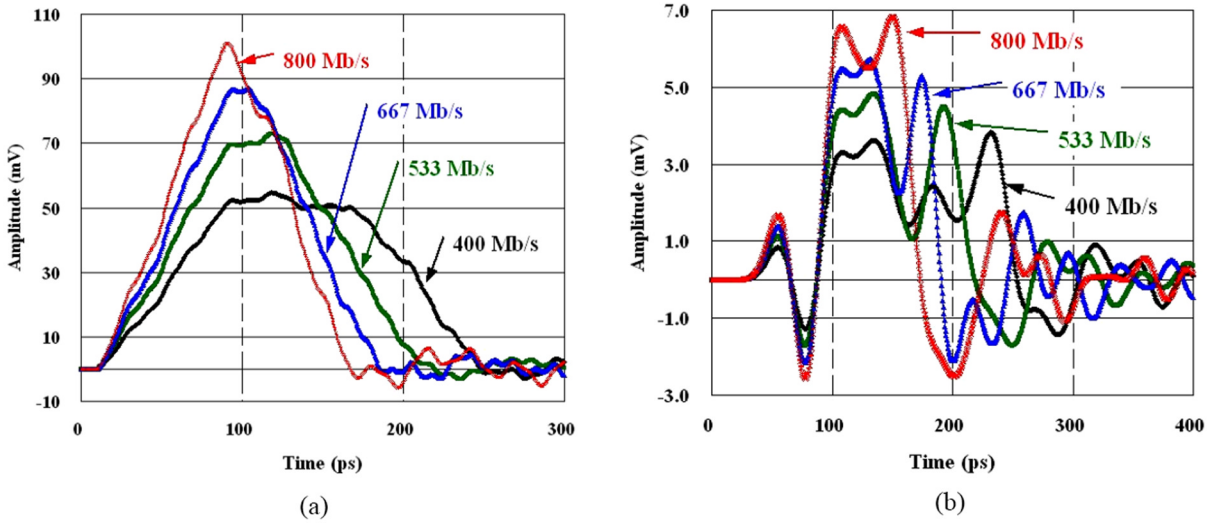

Fig. 12. Voltage waveforms of crosstalk for different pulse speeds. (a) NEXT. (b) FEXT. (Color version available online at http://ieeexplore.ieee.org.)

TABLE III
COMPARISON OF TRANSIENT CHARACTERISTICS FOR COHS-LF AND BGA PACKAGES

Package Type	Net Name	Delay (ps)	T_r (ps)	T_f (ps)	NEXT (mV)	NEXT (%)	FEXT (mV)	FEXT (%)
BGA	DQ3	66.5	119.0	121.0	Active line			
	DQ4	67.5	140.0	140.0	192	10.7	-25	1.4
COHS-LF	Lead7	40.0	63.0	63.0	Active line			
	Lead8	40.5	62.0	63.0	101	5.6	7	0.4

TABLE IV
DELAYS AND CROSSTALK FOR COHS-LF PACKAGE APPLIED TO DIFFERENT DATA PEEDS

Vin		Measured from SPICE			
Speed (Mb/s)	$T_{r,\,0\text{-}100\%}$ (ps)	Net Name	Delay (ps)	NEXT (mV)	FEXT (mV)
400	156.0	**Lead7**	41.5	Active line	
		Lead8	40.5	54.7	3.62
533	117.0	**Lead7**	39.5	Active line	
		Lead8	39.0	72.9	4.83
667	94.0	**Lead7**	39.5	Active line	
		Lead8	39.5	87.0	5.73
800	78.0	**Lead7**	40.0	Active line	
		Lead8	40.5	101.0	6.84

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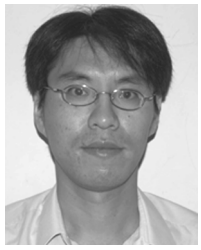

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